IN THE CLAIMS

Please cancel claims 1-44 without prejudice.

Please add claims 45-88 as follows:

~~Patent Claims~~WHAT IS CLAIMED IS:

1-44. (Cancelled)

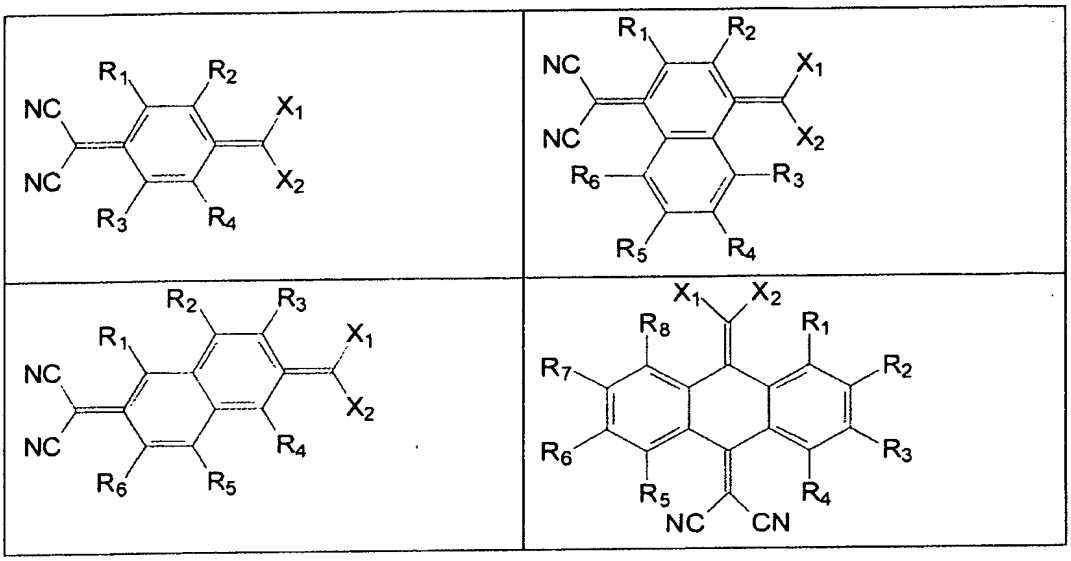
45. (New) A semiconductor arrangement comprising at least one nonvolatile memory cell with a first electrode comprising at least two layers and an organic material, the organic material forming a compound with that layer of the first electrode which is in direct contact, the semiconductor arrangement produced by:

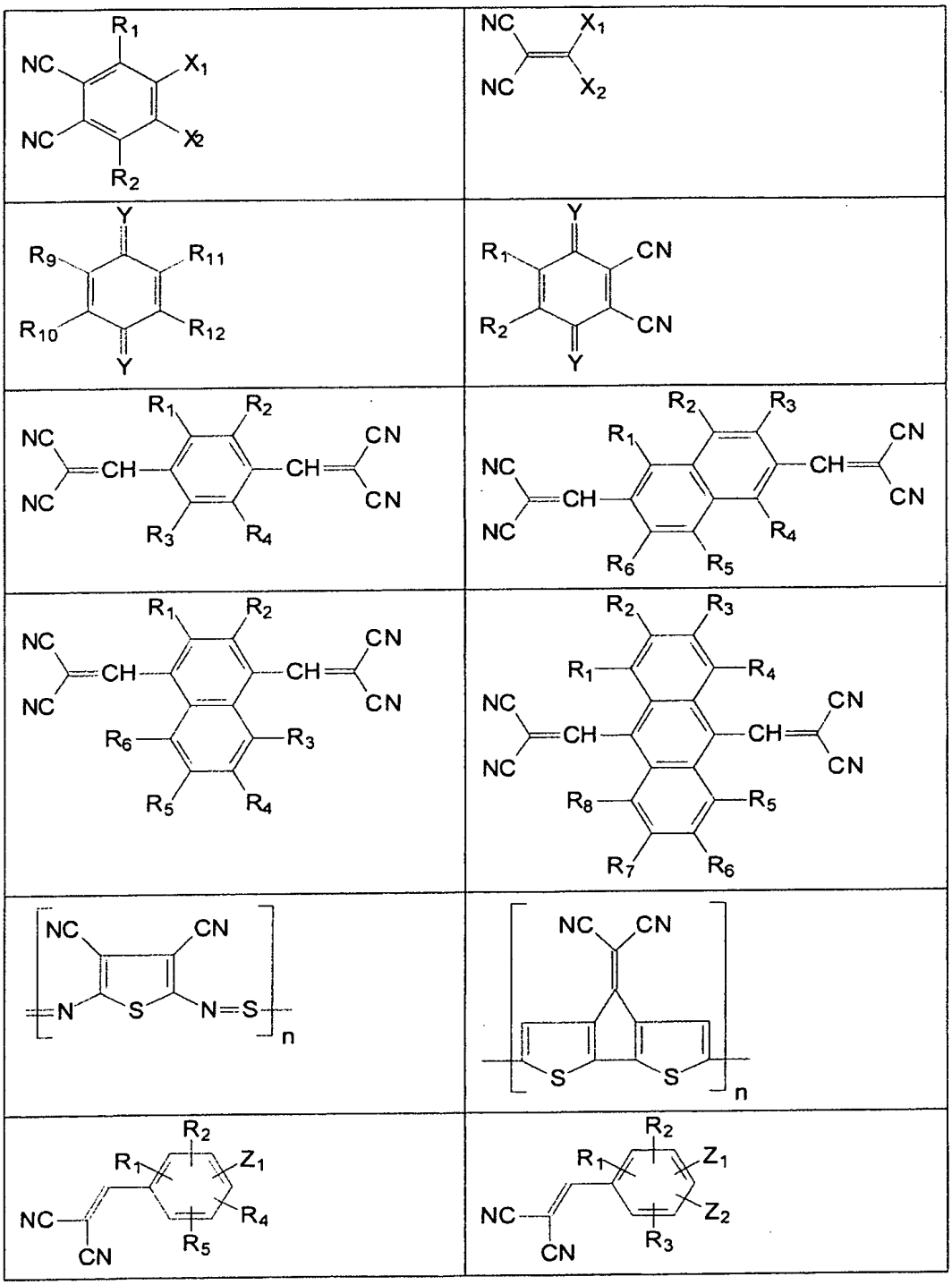
providing a first electrode comprising at least two layers and a layer of the first electrode forms a compound with an organic material;

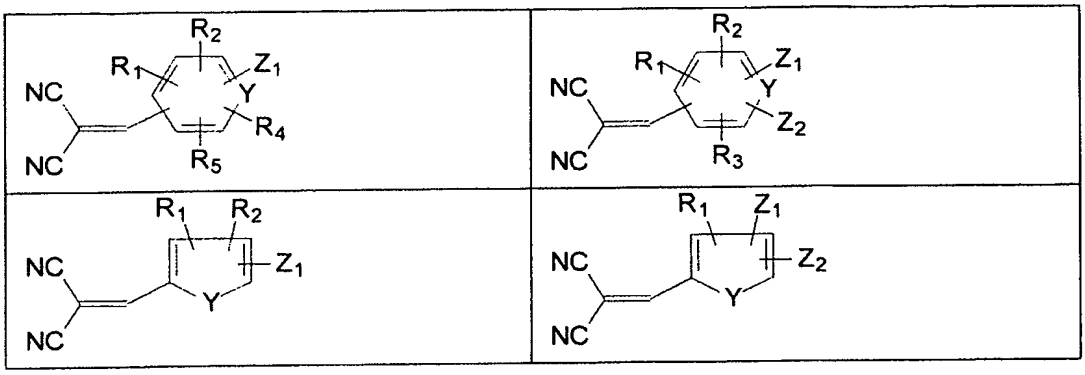
contacting the first electrode with an organic material in order to form a compound; and

forming a second electrode on the compound formed.

46. (New) The semiconductor arrangement of claim 45, wherein the organic material has at least one of the following materials or compounds: sulfur, selenium and tellurium either in pure or in bonded form in particular as organocompounds of sulfur, selenium and tellurium, and sulfur-, selenium- and tellurium-containing oligomers or polymers, and one of the following compounds:

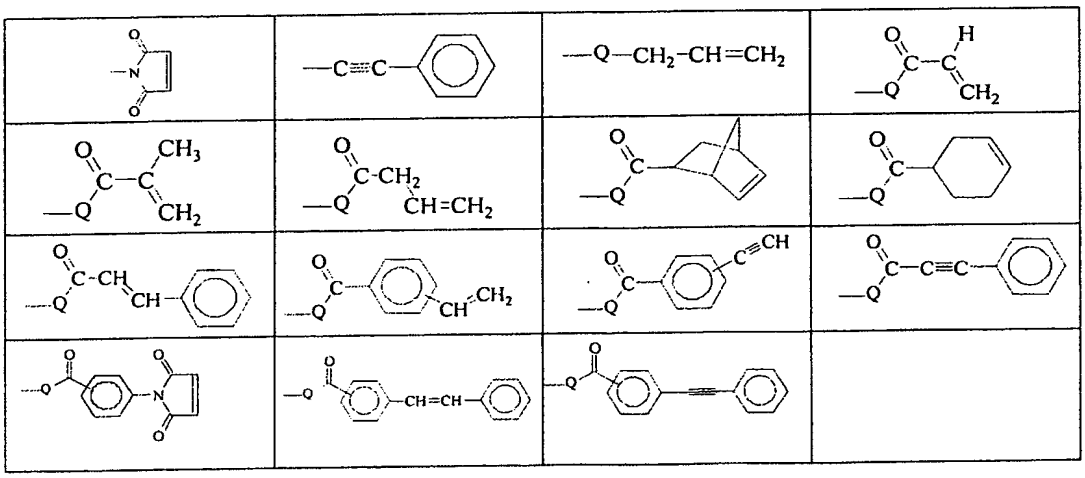

R1
R2
NC
X1
NC
X2
R3
R4
R1
R2
NC
X1
NC
X2
R6
R3
R5
R4
R2
R3
R1
X1
NC
X2
NC
R4
R6
R5
X1
X2
R8
R1
R7
R2
R6
R3
R5
R4
NC
CN





where R_1, R_2, R_3, R_4, R_5, R_6, R_7 and R_8, independently of one another, have the following meaning:

H, F, Cl, Br, I (iodine), alkyl, alkenyl, alkynyl, O-alkyl, O-alkenyl, O-alkynyl, S-alkyl, S-alkenyl, S-alkynyl, OH, SH, aryl, heteroaryl, O-aryl, S-aryl, NH-aryl, O-heteroaryl, S-heteroaryl, CN, NO_2, $-(CF_2)_n-CF_3$, $-CF((CF_2)_nCF_3)_2$, $-Q-(CF_2)_n-CF_3$, $-CF(CF_3)_2$, $-C(CF_3)_3$ and



n: n = 0 to 10

Q: -O-, -S-

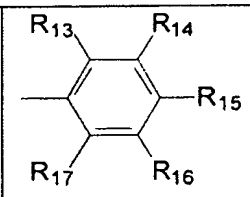
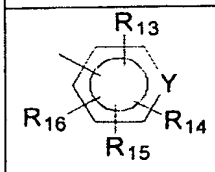
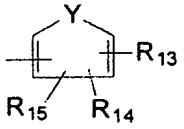
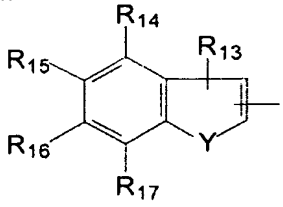
R_9, R_{10}, R_{11}, R_{12} may, independently of one another, be:

F, Cl, Br, I, CN, NO_2

R_{13}, R_{14}, R_{15}, R_{16}, R_{17} may, independently of one another, be:

H, F, Cl, Br, I, CN, NO_2

X_1 and X_2 may, independently of one another, be:

CN	
	
	

Y is: O, S, Se

and Z_1 and Z_2, independently of one another, are: CN, NO_2.

47. (New) The semiconductor arrangement of claim 45, wherein the organic material is an electron acceptor.

48. (New) The semiconductor arrangement of claim 47, wherein the electron acceptor has electron-attracting atoms or groups which are selected from: -Cl, -F, -Br, -I, -CN, -CO-, -NO_2.

49. (New) The semiconductor arrangement of claim 45, wherein the organic material forms a charge transfer complex with the bottom electrode.

50. (New) The semiconductor arrangement of claim 45, wherein that layer of the first electrode which is in contact with the organic material contains one of copper and silver.

51. (New) The semiconductor arrangement of claim 45, wherein the organic material is present in a film thickness of between 30 and 1000 nm.

52. (New) The semiconductor arrangement of claim 45, wherein the cell is scalable up to an area of 40 nm^2.

53. (New) The semiconductor arrangement of claim 45, wherein that layer of the first electrode which is not in contact with the organic material is titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a combination of said layers and/or materials and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC or SiCN.

54. (New) The semiconductor arrangement of claim 45, wherein the second electrode is made of aluminum, copper, AlCu, AlSiCu, silver (Ag), titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO, or a combination of said layers and/or materials and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC or SiCN.

55. (New) The semiconductor arrangement of claim 45, wherein the cell can be switched between an ON state and an OFF state.

56. (New) The semiconductor of claim 55, wherein the ON and OFF states have different electrical resistances.

57. (New) The semiconductor arrangement of claim 56, wherein the ratio between the ON and OFF states is more than 66.

58. (New) A method for producing a nonvolatile memory cell comprising:
providing a first electrode comprising at least two layers and an organic material;
forming a compound with the organic material and a layer of the first electrode;
contacting the electrode with an organic material in order to form a compound; and
forming a second electrode on the compound formed.

59. (New) The method of claim 58, further comprising vapor depositing the organic material onto the electrode under reduced pressure.

60. (New) The method of claim 58, further comprising dissolving the organic material in a solvent in the process of contacting the first electrode.

61. (New) The method of claim 58, further comprising subjecting the organic material to a thermal treatment prior to forming the second electrode.

62. (New) The method of claim 58, further comprising rinsing the excess organic material with a solvent prior to forming the second electrode.

63. (New) The method of claim 59, wherein the organic material is vapor-deposited at a pressure of between 0.00001 and 200 mbar.

64. (New) The method of claim 58, wherein the the contacting of the organic material takes place at a substrate temperature of between -50°C and 150°C.

65. (New) The method of claim 58, further comprising mixing the organic material in the gas phase with a carrier gas.

66. (New) The method of claim 58, further comprising treating the compound formed with an aftertreatment reagent prior to providing the second electrode.

67. (New) The method of claim 66, wherein the aftertreatment reagent is selected from a group comprising: amines, amides, ethers, ketones, carboxylic acids, thioethers, esters, aromatics, heteroaromatics, alcohols and sulphur- and selenium-containing compounds.

68. (New) The method of claim 67, wherein the sulphur-containing compounds are selected from a group comprising: sulphur hetercyclic compounds, -SO- containing compounds and thiols.

69. (New) The method of claim 66, wherein the aftertreatment reagent is selected from the group comprising: diethylamine, triethylamine, dimethylaniline, cyclohexylamine, diphenylamine, dimethylformamide, dimethylacetamide, dimethyl sulfoxide, acetone, diethylketone, diphenylketone, phenyl benzoate, benzofuran, N-methylpyrrolidone, gamma-butyrolactone, toluene, xylene, mesitylene, naphthaline, anthracene, imidazole, oxazole, benzimidazole, benzoxazole, quinoline, quinoxaline, fulvalene, furan, pyrrole, thiophene and diphenyl sulfide.

70. (New) The method of claim 66, wherein the aftertreatment reagent is present in a solution.

71. (New) The method of claim 66, wherein the aftertreatment reagent is present as vapor.

72. (New) The method of claim 66, wherein the aftertreatment time is between 15 seconds and 15 minutes.

73. (New) The method of claim 66, wherein the aftertreatment takes place at a temperature of -30°C to 150°C.

74. (New) The method of claim 66, wherein in the process of contacting the first electrode with the organic material, the aftertreatment reagent is admixed with the solution containing the organic material or with the vapor containing the organic material.

75. (New) The semiconductor arrangement of claim 45, wherein the compound is treated with an aftertreatment reagent and a reaction product of the aftertreatment reagent with the organic material or the electrode material.

76. (New) A semiconductor arrangement with a bit line and a word line having a nonvolatile memory cell with a first electrode comprising at least two layers and an organic material, the organic material forming a compound with that layer of the first electrode which is in direct contact, wherein the nonvolatile memory cells are situated directly between bit and word lines that cross one another.

77. (New) The semiconductor arrangement of claim 76, wherein the nonvolatile memory cells are present in a plurality of layers.

78. (New) The semiconductor arrangement of claim 76, produced by the following steps in any desired order:

forming at least one first interconnect on a substrate, which serves as first electrode;

depositing an insulating layer;

patterning the insulating layer, so that in the insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied;

depositing an organic material; and

depositing at least one second electrode, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell.

79. (New) The semiconductor arrangement of claim 78, wherein the deposition of the insulating layer is effected after the deposition of the organic material.

80. (New) The semiconductor arrangement of claim 77, produced by the following steps in this order:

forming at least one first interconnect on a substrate;

depositing an insulating layer;

patterning the contact holes above the first electrode;

depositing an organic material into the contact holes over the first electrode;

depositing a second insulating layer;

patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array; and

depositing at least one second interconnect, which serves as a second electrode for the memory cell.

81. (New) The semiconductor arrangement of claim 76, produced by a Cu damascene technique.

82. (New) A method for producing a semiconductor arrangement comprising:

forming at least one first interconnect on a substrate, which serves as a first electrode for a memory cell;

depositing an insulating layer;

patterning the insulating layer, so that in insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied;

depositing an organic material;

depositing at least one second electrode, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell.

83. (New) The method of claim 82, further comprising effecting the deposition of the insulating layer after the deposition of the organic material.

84. (New) A method for producing a semiconductor arrangement comprising:

applying at least one first interconnect on a substrate;

depositing an insulating layer;

patterning the contact holes above the first electrode;

depositing an organic material into the contact holes over the first electrode;

depositing a second insulating layer;

patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array; and

depositing at least one second interconnect, which serves as a second electrode for the memory cell.

85. (New) The method of claim 84, further comprising depositing a protective layer on the organic material after the deposition of the organic material prior to further processing.

86. New) The semiconductor arrangement of claim 45 configured as a memory device containing a plurality of the nonvolatile memory cells.

87. (New) The semiconductor arrangement of claim 86, wherein a plurality of memory cells are arranged in one plane.

88. (New) The semiconductor of claim 87, wherein a plurality of memory cells are arranged in the XY plane and in the XZ or YZ plane.